IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A data processing apparatus configured to perform a pipeline processing by dividing a pipeline into a plurality of stages, comprising:

a first pipeline processing portion configured to perform the processing in a plurality of stages in sequence based on a plurality of control signals provided corresponding to the respective stages, said control signals having timings ~~capable of being individually controlled~~ asynchronous to each other;

a first latch portion configured to latch said control ~~signal~~ signals inputted to ~~each stage~~ the respective stages with a predetermined clock, said first latch portion having a plurality of flip-flops which are provided corresponding to the respective control signals and latch the corresponding control ~~signal~~ signals; and

a second pipeline processing portion, disposed separately from said first pipeline processing portion, configured to perform the processing in ~~each stage~~ a plurality of stages in sequence based on the control signal latched by said first latch portion.

Claim 2 (Previously Presented): The data processing apparatus according to claim 1, wherein said control signals are signals for controlling whether or not the pipeline processing is stalled.

Claim 3 (Original): The data processing apparatus according to claim 1, further comprising second latch portion configured to latch a processing result in at least one stage in said first pipeline processing portion with said predetermined clock,

wherein said second pipeline processing portion utilizes data latched by said second

latch portion to perform the processing in the stage corresponding to the data latched by said

second latch portion.

Claim 4 (Original): The data processing apparatus according to claim 1, further

comprising:

a third latch portion configured to latch a processing result in at least one stage in said

second pipeline processing portion with said predetermined clock; and

a selector configured to select either one of data before latched by said third latch

portion and data latched by said third latch portion,

wherein said selector selects a latch output of said third latch portion after the

completion of stall and transmits the latch output to said first pipeline processing portion, if

said first pipeline processing portion is stalled when the processing result in said second

pipeline processing portion is transmitted to said first pipeline processing portion, and selects

the processing result in said second pipeline processing portion and transmits the processing

result to said first pipeline processing portion, when said first pipeline processing portion is

not stalled.

Claim 5 (Previously Presented): The data processing apparatus according to claim 1,

wherein said latch portion latches said control signal with a clock for discriminating the

respective stages.

Claim 6 (Previously Presented): The data processing apparatus according to claim 1,

wherein said second pipeline processing portion performs the pipeline processing one cycle

or more later than a clock for discriminating the stages of said first pipeline processing

portion.

Claim 7 (Previously Presented): The data processing apparatus according to claim 1,

wherein said second pipeline processing portion performs the pipeline processing one cycle

or less than a clock for discriminating the stages of said first pipeline processing portion.

Claim 8 (Previously Presented): The data processing apparatus according to claim 1,

wherein one of said first and second pipeline processing portions includes an integer

operation unit, and the other includes an operation unit other than the integer operation unit.

Claim 9 (Currently Amended): A data processing method for performing first and

second pipeline processings by dividing a pipeline into a plurality of stages, comprising steps

of:

performing said first pipeline processing in a plurality of stages in sequence based on

a plurality of control signals provided corresponding to the respective stages, said control

signals having timings ~~capable of being individually controlled~~ asynchronous to each other;

performing a first latch processing to latch said control ~~signal~~ signals inputted to ~~each~~

~~stage~~ the respective stages with a predetermined clock, said first latch processing latching

said plurality of control signals by using a plurality of flip-flops provided corresponding to

the respective control signals; and

performing a second pipeline processing ~~for each stage~~ in a plurality of stages in

sequence based on said latched control signal separately from said first pipeline processing.

Claim 10 (Previously Presented): The data processing method according to claim 9, wherein said control signals are signals for controlling whether or not the pipeline processing is stalled.

Claim 11 (Original): The data processing method according to claim 9, further comprising a step of performing a second latch processing to latch a processing result in at least one stage in said first pipeline processing with said predetermined clock,

wherein said second pipeline processing comprises a step of utilizing data latched by said second latch processing, when performing the processing in the stage for the data latched by said second latch processing.

Claim 12 (Original): The data processing method according to claim 9, further comprising steps of:

performing a third latch processing to latch a processing result in at least one stage in said second pipeline processing with said predetermined clock; and

selecting either one of data before latched by said third latch processing and data latched by said third latch processing,

wherein said selecting step includes steps of: selecting a latch output of said third latch processing after the completion of stall and transmitting the latch output to said first pipeline processing, when the processing result in said second pipeline processing is transmitted to said first pipeline processing and said first pipeline processing is stalled; and selecting the processing result in said second pipeline processing and transmitting the processing result to said first pipeline processing, when said first pipeline processing is not stalled.

Claim 13 (Previously Presented): The data processing method according to claim 9, wherein said first latch processing comprises a step of latching said control signal with a clock for discriminating the respective stages.

Claim 14 (Previously Presented): The data processing method according to claim 9, wherein said second pipeline processing performs the pipeline processing one cycle or more later than a clock for discriminating the stages of said first pipeline processing.

Claim 15 (Previously Presented): The data processing method according to claim 9, wherein said second pipeline processing performs the pipeline processing one cycle or less than a clock for discriminating the stages of said first pipeline processing.